

IN THE CLAIMS

1-17 (Canceled).

18. (Previously Presented) A data processor comprising:

 a CPU for outputting a first address;
 address translation means for inputting said first address, translating said first address to a second address, and outputting said second address; and

 external bus control means for inputting said second address and outputting said second address to an external device,

 wherein said address translation means has an address translation buffer, a register, and selection means, said address translation buffer stores a first external device control information for controlling said external device in association with either said first address or said second address,

 said register has a second external device control information, and

said selection means selects either said first external device control information or said second external device control information and outputs a selected information to said external bus control means.

19. (Previously Presented) A data processor according to claim 18, wherein said external device is a device having a PCMCIA interface, and

 each of said first external device control information and said second external device control information is an information which specifies at least one of an access timing, a memory attribute, or a bus width of said external device.

20. (Previously Presented) A data processor according to claim 18, wherein said first selection means outputs said second external device control information stored in said register to said external bus control means when said address translation buffer is not used.

21. (Previously Presented) A data processor according to claim 18, wherein said address translation means further comprises an address decoder for receiving said first address; and

 said first selection means selects either said first external device control information or said second external device control information based on a result of decoding of said address decoder and outputs a selected information to said external bus control means.

22-39. (Canceled).